

Modified design for Full Swing SERF and High Speed SERF

Pawan Kumar Mishra, Ms. Himani Mittal

M.Tech (VLSI Design) Department of ECE JSSATE, Noida, UP (India)

Pursuing Ph.D, M.Tech, B.Tech Department of ECE JSSATE, Noida, UP (India)

Abstract

In this chapter we have discussed the research work done on the basis of literature review and study. The research methodology and the techniques to modify the present designs in order to achieve better performance have been discussed with their merits and demerits. In this paper FS-SERF and HS- SERF full adder topologies are presented. The analysis of Power, Delay, Power Delay Product (PDP) optimization characteristics of SERF Adder is designed. In order to achieve optimal power savings at smaller geometry sizes, proposed a heuristic approach known as FS-SERF and HS-SERF adder model.

Index Terms– SERF, 1-bit full adder low, Power Delay Product and Adders.

I. INTRODUCTION

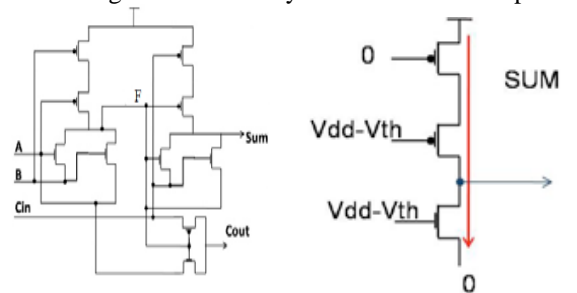
Power consumption is a key limitation in many electronic systems, ranging from mobile telecom to portable and desktop computing systems. Power is also a show stopper for many emerging applications like ambient intelligence and sensor networks. Consequently, new design techniques and methodologies are needed to control and limit power consumption. From sophisticated handheld devices to bioelectronics circuits and nano-satellites, all require low power design. Due to scaling, circuits are becoming more capable, use more transistors to implement complicated functions and offer new applications to customers. But this means more power consumption. In some cases, low power design is required to avoid over heating. There are other applications like bioelectronics where the circuit would be implanted inside the body and has to work either with small battery or using power harvesting techniques. Similar to that, RFID and growing sensor networking circuits also have to consume very low power because of available power limitation. In some cases we may consider low-power design a second priority, but in those applications lower-power design is critical. So either source power limitation or, over heating concern and battery life consideration, low power design is the answer.

In digital processing, a full adder is one of the main elements; an ALU, DSP and digital filtering in any microprocessor/microcontroller are based on it. Therefore, to have low power digital processing, a low-power full adder is desired.

II. SERF ADDER MODEL

In Static Energy Recovery Full (SERF) adder is proposed, which requires only 10 transistors to implement a full adder. This adder makes use of the

design architecture shown in Fig where an intermediately generated *XNOR (A,B) signal is shared* to generate the carry out and the sum outputs.



a) SERF Adder b) Equivalent ABCin= "110"

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	Vdd-Vth	≅0
0	1	0	1	Vtp
0	1	1	0	1
1	0	0	1	>Vtp
1	0	1	0	1
1	1	0	Power consuming (is shown in Fig.3) causes failure	Vdd-2Vth (Fig.1)
1	1	1	>Vdd-2Vth	Vdd-Vth

Truth table of SERF full adder design

III. MODIFIED SERF MODEL

To modify the SERF full adder for different inputs, we add an extra circuit to the SERF adder as shown in Figure 1. By adding this circuit to the SERF, the F node voltage for input vectors ABC

in="110", "111"), is connected to VDD, which increases the output by V_{th} , so we can scale the supply voltage to $V_{tn}+V_{tp}$ that is estimated to be lower than 0.3V instead of 0.45V for SERF full adder.

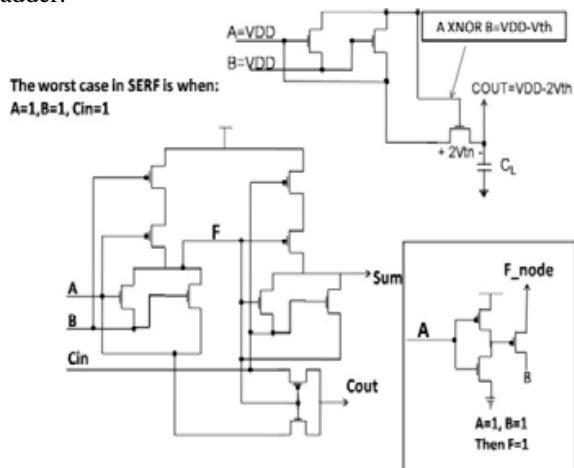


Figure 1

IV. RELATED WORKS

Full swing design SERF

The first design has been optimized for full scale output swing as it is a desirable property in multi bit adders because of the decay in signal level as it propagates through multiple stages. This design consumes low power and has a larger delay than HS-SERF.

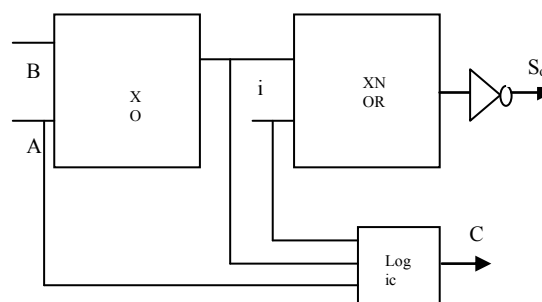
High speed SERF as the name suggests is a high speed structure and is optimum for high frequency systems. It consumes more power than the FS-SERF. Both of the designs show improved results in comparison to present design of modified SERF.

The chapter is divided into different parts. The chapter starts with description of proposed designs separately. Then comparison of designs with previous designs is carried out along with discussions on the results of modified SERF and the proposed designs obtained from simulations. The chapter ends with conclusion based on the results and comparisons. The future scope of improvement in the design is also included in the last section.

This design provides 0 to VDD swing irrespective of the drop of V_{th} across pass transistors in previous stages. Full swing at Sum output makes it ideal for ripple carry adders and tree structure. (FS also eliminates need of buffer at Sum output). The design uses 12 transistors. The second stage (XNOR) has been replaced by XOR and optimized to obtain right logic With minimum delay.

The modified designs have been obtained by using the inverter to restore the level and XNOR/XOR and inverter to implement the logic for sum. A custom logic has been used to implement the

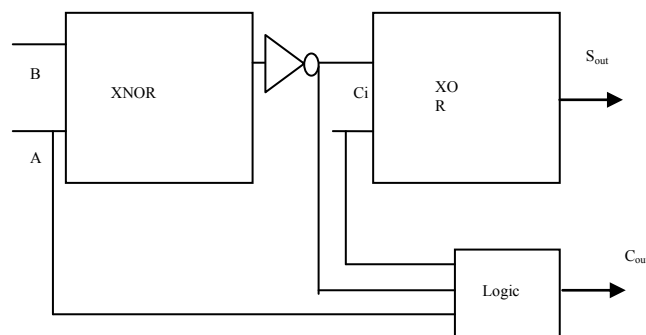
carry logic. The logic block diagrams of two designs are given below.



Logic diagram of FS-SERF

High speed design SERF

The design has highest logic low level and lowest logic high level of V_{tp} and $V_{dd} - V_{th}$ because of restored levels at intermediate node. Design has short propagation delay due to level restoration at node F, and is good for comparatively high speed applications. Design. The minimum logic high voltage has been restored to VDD by using inverter at intermediate node F. The first XNOR has been replaced by 4 transistor XOR gate.



Logic diagram of HS-SERF

As we can see in the schematic above, there is an inverter between the XOR and XNOR block. It makes the design better in following ways:

The inverter restores the logic levels and there is no partially on PMOS because of the restored levels.

It speeds up the charging of the intermediate nodes for all the input combinations thus improving the speed in comparison to the case of modified SERF.

The two designs are not only different in arrangement of logical blocks but also differ in sizing of the MOSFETs. The width of the devices has been set in order to achieve the desired results and width appropriate for the particular design is found by multiple iterations of simulation and resizing.

V. SIMULATION SETUP

Power consumption is very important factor for any circuit design

$$P_{avg} = \alpha C_L V_{DD}^2 f \quad \text{----- (2)}$$

Where,

C is the load capacitance, α is the switching activity, f is the clock frequency, V_{DD} is the supply voltage of the system, I_{sc} is the short circuit current and I_{leak} is the leakage current of the circuit.

The Effective gate length, Gate oxide thickness, Threshold

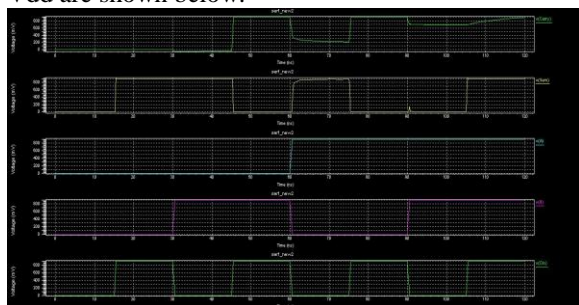
Voltage, Drain Source parasitic resistance are the important parameter in low power design. The technology models 65 nm are used for simulations.

VI. SIMULATION RESULTS

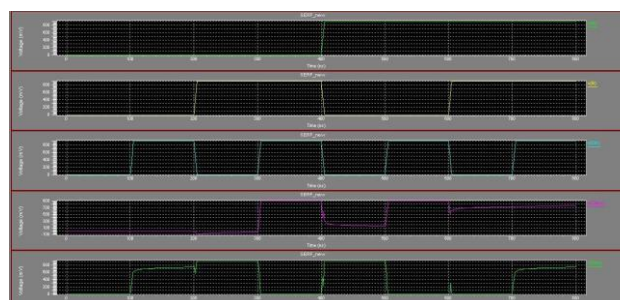
In this section, performance measurement Comparison of different parameters of SERF, Modified SERF, FS-SERF, HS-SERF at 65nm is given in the following table. The design constraints were the same for all the adders. Though low power is the objective of our design, we wanted to measure the delay and power of these circuits, as they are indicators of good performance.

Parameter	SERF	Mod. SERF	FS-SERF	HS-SERF
Power (uw)	1.56	1.41	0.84	1.01
Delay (pS)	145	118	84	72
Device count.	10	13	12	12
Swing drop*	Vdd-2Vth	Vdd-Vth	Vdd	Vdd-Vth
PDP (18)	93	84	71	73

The waveforms obtained from simulation of the designs at 100MHz input frequency and 0.9 volts V_{DD} are shown below.



Simulation waveforms of FS-SERF



Simulation waveforms of HS-SERF

Low-voltage performance of FS-SERF and HS-SERF

The two proposed provide accurate logic levels at voltages as low as 0.3 Volts. In sub-threshold operation the power consumption reduces further at the cost of delay, as the sub threshold circuits are slow due to the dependence of operation on leakage currents only. The design can be operated at maximum frequency of 100MHz at 0.3 V. Increase speed can be achieved by increasing V_{DD} . The waveforms obtained from simulation of designs at 0.3V

VII. CONCLUSIONS

Both the designs show lower power consumption and a better PDP in comparison to SERF and Mod. SERF. FS-SERF consumes lesser power than HS-SERF due to lower intermediate voltages, but this makes the design slow too. HS-SERF due to level restoration at node F shows a short propagation delay and also consumes more power than FS-SERF. From the simulation waveforms of FS-SERF and HS-SERF at sub-threshold voltage we can conclude that the FS-SERF has a more stable behaviour than FS design. Depending on application we can choose on of the proposed design for best performance. This work primarily focused on the design of low power and high performance adder.

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